**Modeling the Rise and Fall Times of a Digital Logic Circuit Using the Logistic Function**

***Digital Logic Circuits***

Digital logic circuits are used to process data that is stored in binary format. Depending on the specific family of logic circuit that is considered, a binary value of “1” is stored as a voltage of 5 V. A binary value of “0” is stored as a voltage of 0 V.

At various times, the state of a binary variable will change from “0” to “1” and from “1” to “0”. The amount of time that the output of a logic circuit takes to change from one state to another is called the ***transition time***.

Consider the Figure below. The plot (a) shows how we might like digital outputs to change state. Here, the change of state is accomplished in zero time. It represents what is known as the ***ideal case***. 

From a physical standpoint, the output of a real digital circuit cannot change state instantaneously. Instead, a more realistic view of a circuit’s output is shown in (b). Here we observe that there is a finite time, *tr*, that it takes for the output of the digital circuit to rise from the LOW state to the HIGH state. This value, *tr*, is called the ***rise time***. There is a finite time, *tf*, which is called the ***fall time*** that is associated with the fall of an output of from the state HIGH to the state LOW.

Even the situation shown in (b) is not entirely accurate. Figure (b) is just a linear approximation to what happens in the real world.

A more realistic representation is shown in Figure (c). In Figure (c), the output voltage at the beginning and the end of a transition between logic states is smooth.

***Transistor Transistor Logic Family***

The most frequently encountered digital logic circuits come from the Transistor Transistor Logic (TTL) family. Such circuits are built from bipolar junction transistors and resistors. The family is called transistor-transistor logic because both the logic gating function and the amplifying function are performed by transistors.

Digital logic circuits from the TTL family represent Logic “1” (HIGH) ideally as a voltage of value 5 Volts. Practically speaking any output voltage in excess of 3.5 Volts is declared as Logic “1”. A Logic “0” (LOW) is ideally represented by a voltage of 0 Volts. In practice, any output voltage less than 1.5 Volts is declared as Logic “0”. The rise time and fall time for a TTL circuit are the same, 50 ns.

Let us re-examine Figure (c), the rise time and the fall time indicate how long an output voltage takes to pass through the “undefined” region between the LOW state and the HIGH state. Thus, the rise time is equivalent to the amount of time it takes for the output voltage to rise from 1.5 Volts to 3.5 Volts. Conversely, the fall time is equivalent to the amount of time it takes for the output voltage to fall from 3.5 Volts to 1.5 Volts. The initial part of a transition from one state to another is not included in value of the rise- or fall-time. Instead, the initial part of a transition contributes to the value of what is known as the ***propagation delay*** for the digital logic circuit.

***Modeling Using the Logistic Function***

The logistic function is one that can be used to model the behavior of the output voltage of a digital logic circuit. The logistic model may be expressed as follows:

 

The shape of the curve associated with the logistic model is determined in part by the values of the parameters (*L*, *A* and *k*). Figures 4.42 – 4.44 of your text display various plots of the logistic model for different assignments of the parameters (*L*, *A*, and *k*.) 

We can select the parameters (A, L and k) of the logistic function to model TTL circuit behavior.

***Choosing the parameter L***

It should be obvious that we will choose the value of 5 for L. This is so because we wish the maximum value of the logistic function to be close to 5 Volts.

***Choosing the parameter A***

We want the logistic function to take on a value close to 0 at its minimum. This can be achieved by selecting the value of 100 for A. This choice for A will create a minimum value of 0.0495 Volts. This value is very close to the desired value of 0 Volts.

***Choosing the parameter k***

Now we proceed to choosing an appropriate value for the parameter *k*. Our choice will be influenced by the value for the rise and fall time for a transistor-transistor logic circuit. Let us direct our attention to the figure below. It provides some of the labeling information needed in order to follow the derivation of parameter *k*. Because the rise time and the fall time for a TTL logic circuit are equal, we will focus on just the rise time in our pursuit to choose the parameter *k*.



3.5 V

1.5 V

*t1 t2*

**Figure: Rise time and associated quantities for a TTL circuit.**

Let us begin by listing the model we wish to use along with what we know about the rise time of a TTL circuit.



Next, we find relationships involving parameter *k* and the times t*1* and t2. We make use of the fact that voltages less than 1.5 Volts are declared as LOW, while those over 3.5 Volts are declared as HIGH. 

Next, we subtract the term on the left from that on the right.



We then develop an expression for parameter *k*.



We are now ready to make use of the published rise time for TTL logic (50 ns) and solve for parameter k.



Thus we can model the output voltage of a TTL digital logic circuit using the logistic function along with a judicious selection of parameters as below (*L*=5 and *A*=100). 

Extension of the Model

Once a model for the output voltage undergoing a transition from the LOW to the HIGH state is obtained, it is very simple to extend it to the case when the output voltage drops from the HIGH state to the LOW state. Due to the equality of the rise and fall times associated with this class of digital circuits, a fall in voltage can be modeled by subtracting the logistic function from unity. Using the values for the parameters found earlier, a falling voltage can be written as

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